## Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claim in the application:

**Listing of Claims:**

1. (Canceled)

2. (Canceled)

3. (Currently Amended) A family of two or more ASIC devices comprising a processor having mask-programmable instructions implemented in ASIC logic, wherein each device member of the family has different amounts of ASIC logic available, and wherein each member of the device family has substantially identical processors, processor memory, and numbers of input/output connections (I/O), and ~~The ASIC device family of claim 2,~~ wherein all device members of the family are configured to plug into the same socket in a target system and function properly.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Currently Amended) An integrated circuit, comprising:

    a fixed portion comprising one or more fixed logic blocks;

a reprogrammable portion comprising a plurality of reprogrammable logic blocks; and

instruction logic coupled to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks, wherein the instruction logic is configured to decode an instruction stream of a software program to sequentially provide control signals to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks according to a sequence of execution of the software program ~~The integrated circuit of claim 9,~~ and wherein the instruction logic is further configured to wait until the reprogrammable portion returns a result from an operation performed according to an instruction of the software program before providing an immediately subsequent instruction of the software program to the fixed portion.

11. (Currently Amended) The integrated circuit of claim 10~~9~~, wherein the reprogrammable portion is subordinate to the fixed portion.

12. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the fixed portion is a software-programmable digital signal processor (DSP).

13. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the reprogrammable portion is a field-programmable gate array (FPGA).

14. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein substantially all of the plurality of reprogrammable logic blocks are identical.

15. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the plurality of reprogrammable logic blocks include at least two different reprogrammable logic block types that differs by an amount of logic and/or a type of logic.

16. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the reprogrammable portion further comprises at least one application-specific function block.

17. (Previously Presented) The integrated circuit of claim 16, wherein the at least one application-specific function block is a Multiplier, Barrel Shifter, Bit-Reverse Address Generator, Auto-Scaling Unit, Large Multiplier, or Viterbi Decoder.

18. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the fixed portion comprises the instruction logic.

19. (Currently Amended) The integrated circuit of claim ~~9~~10, wherein the instruction logic is at least partially reprogrammable to provide a reprogrammable instruction set.

20. (Previously Presented) The integrated circuit of claim 19, wherein the at least partially reprogrammable instruction logic is configured to perform instruction decoding for at least some of the fixed portion.

21. (Previously Presented) The integrated circuit of claim 19, wherein the at least partially reprogrammable instruction logic comprises:

a content-addressable memory (CAM) configured to accept results signals from the fixed function blocks, the reprogrammable logic blocks, and/or data path elements of the integrated circuit, and to encode the accepted results signals; and

a memory element comprising:

a first set of address inputs, coupled to outputs of the CAM, to receive an encoded signal from the CAM; and

a second set of address inputs, coupled to an instruction fetch logic element of the integrated circuit, to accept instruction signals according to the software program, and to decode the encoded signal to control the plurality of reprogrammable logic blocks and/or the one or more fixed logic blocks.

22. (New) A family of two or more integrated circuit devices, each comprising:

a fixed portion comprising one or more fixed logic blocks; and

a reprogrammable portion comprising a plurality of reprogrammable logic blocks, wherein each device member of the family has different numbers of reprogrammable logic blocks, and wherein each member of the device family has

substantially identical numbers of fixed logic blocks, memory, and numbers of input/output connections (I/O), and wherein all device members of the family are configured to plug into the same socket in a target system and function properly.

23. (New) The family of two or more integrated circuit devices of claim 22, wherein all device members comprise instruction logic coupled to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks, wherein the instruction logic is configured to decode an instruction stream of a software program to sequentially provide control signals to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks according to a sequence of execution of the software program and wherein the instruction logic is further configured to wait until the reprogrammable portion returns a result from an operation performed according to an instruction of the software program before providing an immediately subsequent instruction of the software program to the fixed portion.

24. (New) The family of two or more integrated circuit devices of claim 23, wherein the reprogrammable portions are subordinate to the fixed portion.

25. (New) The family of two or more integrated circuit devices of claim 23, wherein the fixed portions are a software-programmable digital signal processor (DSP).

26. (New) The family of two or more integrated circuit devices of claim 23, wherein the reprogrammable portions are a field-programmable gate array (FPGA).

27. (New) The family of two or more integrated circuit devices of claim 23, wherein substantially all of the plurality of reprogrammable logic blocks of each family member are identical.

28. (New) The family of two or more integrated circuit devices of claim 23, wherein the plurality of reprogrammable logic blocks of each family member include at least two different reprogrammable logic block types that differs by an amount of logic and/or a type of logic.

29. (New) The family of two or more integrated circuit devices of claim 23, wherein the reprogrammable portion of each family member further comprises at least one application-specific function block.

30. (New) The family of two or more integrated circuit devices of claim 29, wherein the at least one application-specific function block is a Multiplier, Barrel Shifter, Bit-Reverse Address Generator, Auto-Scaling Unit, Large Multiplier, or Viterbi Decoder.

31. (New) The family of two or more integrated circuit devices of claim 23, wherein the fixed portion of each family member comprises the instruction logic.

32. (New) The family of two or more integrated circuit devices of claim 23, wherein the instruction logic of each family member is at least partially reprogrammable to provide a reprogrammable instruction set.

33. (New) The family of two or more integrated circuit devices of claim 32, wherein the at least partially reprogrammable instruction logic of each family member is configured to perform instruction decoding.

34. (New) The family of two or more integrated circuit devices of claim 32, wherein the at least partially reprogrammable instruction logic of each family member comprises:

a content-addressable memory (CAM) configured to accept results signals from the fixed function blocks, the reprogrammable logic blocks, and/or data path elements of the integrated circuit, and to encode the accepted results signals; and

a memory element comprising:

a first set of address inputs, coupled to outputs of the CAM, to receive an encoded signal from the CAM; and

a second set of address inputs, coupled to an instruction fetch logic element of the integrated circuit, to accept instruction signals according to the software program, and to decode the encoded signal to control the plurality of reprogrammable logic blocks and/or the one or more fixed logic blocks.